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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/035,864 | 12/26/2001 | Chris Goodings | 2002282 | 4869 |

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| EXAMINER | |
|---|---|
| SWERDLOW, DANIEL | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2644 | |

DATE MAILED: 12/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/035,864 | GOODINGS, CHRIS | |
| | Examiner | Art Unit | |
| | Daniel Swerdlow | 2644 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on 26 December 2001.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 1-22 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-22 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 26 December 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 6/3/03, 9/17/03.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Priority*

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1 through 5, 7, 18 through 20 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Oprea (US Patent 5,323,456).

4. Regarding Claim 1, Oprea discloses controlling volume in a telephone ringer (column 1, lines 37-41) including: establishing a ringing frequency of 348 Hz and 445 Hz (i.e., generating a first signal in the audible frequency range) (column 3, lines 17-19); generating a train of inaudible 128 kHz pulses (i.e., a second signal with a higher frequency than the first signal) (column 3, lines 38-42) and a duty cycle (i.e., mark-space ratio) of 3/16 to 9/16 (i.e., less than 100%) (column 4, lines 55-58); combining (i.e., modulating) the ringing signal frequency (i.e., first signal) with the pulse train (i.e., second signal) in an AND gate (Fig. 1, reference 3; column 3, lines 25-32) to produce an output with the same 348 Hz and 445 Hz frequencies (i.e., similar timbre to the first signal); driving a speaker (i.e., applying the output signal to the audio transducer) (column 1, line 56); whereby the volume is controlled by modifying the pulse width

of the pulses forming the pulse train (i.e., varies with the mark-space ratio of the second digital pulse train signal) (column 1, lines 49-51).

5. Regarding Claim 2, Oprea further discloses the ringing frequency signal (i.e., first signal) being the output of a digital counter and an input of a digital logic AND gate (i.e., a square wave that alternates between high and low logic levels) (column 3, lines 9-22).

6. Regarding Claim 3, Oprea further discloses a duty cycle for the pulse train (i.e., second signal) of 9/16 (i.e., approximately 50%) (column 4, lines 55-58).

7. Regarding Claim 4, Oprea further discloses the pulse train (i.e., second signal) being a train of inaudible 128 kHz pulses (i.e., a frequency above the range of human hearing) (column 3, lines 38-42).

8. Regarding Claim 5, Oprea further discloses that the 128 kHz pulses (i.e., second signal) are not reproduced in the voice coil of the loudspeaker (i.e., the frequency is greater than the cutoff frequency of the audio transducer) (column 6, lines 61-64).

9. Regarding Claim 7, Oprea discloses controlling volume in a telephone ringer (column 1, lines 37-41) including: a controller (Fig. 1, reference 6; column 3, lines 1-5) that provides a binary count value that determines the action of a volume control (Fig. 1, reference 2) (i.e., selecting a desired ring volume level); a frequency control circuit (Fig. 1, reference 7; column 3, lines 9-20) that produces a ringing frequency of 348 Hz and 445 Hz (i.e., generating a full volume telephone ringing signal); combining in an AND gate (i.e., multiplying) (Fig. 1, reference 3; column 3, lines 25-32) the ringing signal frequency (i.e., full volume ringing signal) and a train of inaudible 128 kHz pulses with a duty cycle of 3/16 to 9/16 (i.e., a pulse train signal with a mark-space ratio less than 100%) to generate an output signal (column 3, lines 26-33),

where the pulse length and repetition rate (i.e., mark-space ratio) of the repetitive pulse (i.e., pulse train) signal is determined by (i.e., dependent upon) the binary count value selected by the controller (i.e., the selected desired ring volume level) (column 3, lines 1-5); driving a speaker (i.e., applying the output signal to an audio transducer) (column 1, line 56); to produce an output with the same 348 Hz and 445 Hz frequencies (i.e., similar timbre to the first signal) (column 3, lines 25-32) with controlled (i.e., reduced) volume (column 1, lines 49-51).

10. Regarding Claim 18, Oprea discloses controlling volume in a telephone ringer (i.e., an audible alert circuit) (column 1, lines 37-41) including: a frequency control circuit (Fig. 1, reference 7; column 3, lines 9-20) that produces a pulse (i.e., square wave) signal at the ringing frequency (i.e., tone) (Fig. 5, reference C; column 6, lines 44-48); a volume control (i.e., digital pulse train generator) (Fig. 1, reference 2) generating a train of 128 kHz pulses (column 3, lines 38-42) with a duty cycle (i.e., mark-space ratio) of 3/16 to 9/16 (i.e., less than 100%) (column 4, lines 55-58) using pulse width modulation (column 1, lines 49-51); an AND gate (i.e., multiplier) (Fig. 1, reference 3; column 3, lines 1-5, 20-21) to which the outputs of the frequency control circuit (i.e., tone generator) and the volume control (i.e., digital pulse train generator) are applied; a loudspeaker (i.e., audio transducer) (Fig. 1, reference 5, column 2, lines 53-54) connected to the AND gate (i.e., multiplier) output; whereby the volume of the ringing (i.e., alert) signal is controlled by modifying the pulse width of the pulses forming the pulse train (i.e., is determined by the mark-space ratio of the pulse train signal) (column 1, lines 49-51).

11. Regarding Claim 19, Oprea further discloses the pulse train (i.e., second signal) being a train of inaudible 128 kHz pulses (i.e., a frequency above the range of human hearing) (column 3, lines 38-42).

12. Regarding Claim 20, Oprea further discloses that the 128 kHz pulses (i.e., second signal) are not reproduced in the voice coil of the loudspeaker (i.e., the frequency is greater than the cutoff frequency of the audio transducer) (column 6, lines 61-64).

13. Regarding Claim 22, Oprea further discloses the multiplier being an AND gate (Fig. 1, reference 3; column 3, lines 1-5, 20-21).

***Claim Rejections - 35 USC § 103***

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Oprea in view of Hsu (US Patent 5,802,187).

16. Regarding Claim 6, as shown above apropos of Claim 1, Oprea anticipates all elements except the frequency of the digital pulse train signal being approximately 64 kHz. Hsu discloses a pulse width controlled volume controllable that derives a 64 kHz pulse train of variable duty cycle (Fig. 6) from a 64 kHz clock and a 128 kHz clock (Fig. 5, reference HZ64K, HZ128K) using only four NAND gates and two inverters (Fig. 5, reference 611-616; column 6, lines 9-18). Note that the output of gate 614 when it is enabled by control signals VOL[1] and VOL[0] is the 64 kHz clock HZ64K and the output of gate 614 when it is enabled by control signals VOL[1] and VOL[0] is the Boolean product of 64 kHz clock HZ64K and 128 kHz clock HZ128K which is a 64 kHz pulse train of narrower pulse width. As such, the pulse train generation circuit taught

by Hsu uses fewer components than the one used by Oprea (Fig. 2). Oprea discloses the desirability of reducing the number of logic gates used in the design (column 1, lines 57-61). Oprea further discloses that any pulse train frequency an order than the ringer audio frequency is suitable (column 2, lines 10-15). As such, it would have been obvious to one skilled in the art at the time of the invention to apply the 64 kHz pulse train generator taught by Hsu to the ringer volume control taught by Oprea for the purpose of reducing the size, cost and power consumption of the device by reducing the number of logic gates.

17. Claims 8 through 11, 13 through 15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oprea in view of Yeh (US Patent 4,644,106).

18. Regarding Claim 8, Oprea discloses a ringing generator for use in a telephone (i.e., a telephone that can produce a ringing signal) (column 1, lines 6-8) that produces a signal of varying volume (column 1, lines 37-39) comprising: a frequency control circuit (i.e., tone generator) (Fig. 1, reference 7; column 3, lines 9-20) that produces a pulse signal at the ringing frequency (i.e., a telephone ring signal) (Fig. 5, reference C; column 6, lines 44-48); a volume control (i.e., digital pulse train generator) (Fig. 1, reference 2) generating a train of 128 kHz pulses (column 3, lines 38-42) with a duty cycle (i.e., mark-space ratio) of 3/16 to 9/16 (i.e., less than 100%) (column 4, lines 55-58) using pulse width modulation (column 1, lines 49-51) based on a binary count value from a controller (Fig. 1, reference 6; column 3, lines 1-5); an AND gate (i.e., switch) (Fig. 1, reference 3; column 3, lines 1-5, 20-21) controlled by the output of the volume control (i.e., digital pulse train generator) to pass the output of the frequency control circuit (i.e., tone generator) when the output of the volume control (i.e., digital pulse train

generator) is true (i.e., a mark); and a loudspeaker (i.e., audio transducer) (Fig. 1, reference 5, column 2, lines 53-54) connected to the AND gate (i.e., switch) output, whereby the output volume is controlled by the binary count value from the controller (column 3, lines 1-5). Therefore Oprea anticipates all elements of Claim 8 except the volume control originating at a user interface. Yeh discloses a keypad (i.e., user interface) (Fig. 2, reference 7; column 3, lines 1-6) used to input sound characteristics (i.e., volume) for a telephone ringing signal. Yeh further discloses such user control of telephone ringer characteristics can avoid much inconvenience to the user and others (column 1, lines 37-45). It would have been obvious to one skilled in the art at the time of the invention to apply the user interface taught by Yeh to the ringing generator taught by Oprea for the purpose of realizing the aforesaid advantages.

19. Regarding Claim 9, Oprea further discloses the ringing frequency signal (i.e., telephone ring signal) being the output of a digital counter and an input of a digital logic AND gate (i.e., a digital signal that alternates between high and low logic levels) (column 3, lines 9-22).

20. Regarding Claim 10, Oprea further discloses the pulse train being a train of inaudible 128 kHz pulses (i.e., above the range of human hearing) (column 3, lines 38-42).

21. Regarding Claim 11, Oprea further discloses that the 128 kHz pulses (i.e., digital pulse train) are not reproduced in the voice coil of the loudspeaker (i.e., the frequency is greater than the cutoff frequency of the audio transducer) (column 6, lines 61-64).

22. Regarding Claim 13, Oprea discloses a ringing generator for use in a telephone (i.e., a telephone that can produce a ringing signal) (column 1, lines 6-8) that produces a signal of varying volume (column 1, lines 37-39) comprising: a frequency control circuit (i.e., tone generator) (Fig. 1, reference 7; column 3, lines 9-20) that produces a pulse signal at the ringing

frequency (i.e., a telephone ring signal comprised of a digital square wave) (Fig. 5, reference C; column 6, lines 44-48); a volume control (i.e., digital pulse train generator) (Fig. 1, reference 2) generating a train of 128 kHz pulses (column 3, lines 38-42) with a duty cycle (i.e., mark-space ratio) of 3/16 to 9/16 (i.e., less than 100%) (column 4, lines 55-58) using pulse width modulation (column 1, lines 49-51) based on a binary count value from a controller (Fig. 1, reference 6; column 3, lines 1-5); an AND gate (i.e., multiplier) (Fig. 1, reference 3; column 3, lines 1-5, 20-21) to which the output of the volume control (i.e., digital pulse train) and the output of the frequency control circuit (i.e., telephone ring signal) are applied; and a loudspeaker (i.e., audio transducer) (Fig. 1, reference 5, column 2, lines 53-54) connected to the AND gate (i.e., switch) output, whereby the output volume is controlled by the binary count value from the controller (column 3, lines 1-5). Therefore Oprea anticipates all elements of Claim 8 except the volume control originating at a user interface. Yeh discloses a keypad (i.e., user interface) (Fig. 2, reference 7; column 3, lines 1-6) used to input sound characteristics (i.e., volume) for a telephone ringing signal. Yeh further discloses such user control of telephone ringer characteristics can avoid much inconvenience to the user and others (column 1, lines 37-45). It would have been obvious to one skilled in the art at the time of the invention to apply the user interface taught by Yeh to the ringing generator taught by Oprea for the purpose of realizing the aforesaid advantages.

23. Regarding Claim 14, Oprea further discloses the pulse train being a train of inaudible 128 kHz pulses (i.e., above the range of human hearing) (column 3, lines 38-42).

24. Regarding Claim 15, Oprea further discloses that the 128 kHz pulses (i.e., digital pulse train) are not reproduced in the voice coil of the loudspeaker (i.e., the frequency is greater than the cutoff frequency of the audio transducer) (column 6, lines 61-64).

25. Regarding Claim 17, Oprea further discloses the multiplier being an AND gate (Fig. 1, reference 3; column 3, lines 1-5, 20-21).

26. Claims 12, 16 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oprea in view of Yeh as applied to Claims 8, 13 and 18, respectively, above, and further in view of Hsu.

27. Regarding Claims 12, 16 and 21, as shown above apropos of Claims 8, 13 and 18, respectively, the combination of Oprea and Yeh makes obvious all elements except the frequency of the digital pulse train signal being approximately 64 kHz. Hsu discloses a pulse width controlled volume controllable that derives a 64 kHz pulse train of variable duty cycle (Fig. 6) from a 64 kHz clock and a 128 kHz clock (Fig. 5, reference HZ64K, HZ128K) using only four NAND gates and two inverters (Fig. 5, reference 611-616; column 6, lines 9-18). Note that the output of gate 614 when it is enabled by control signals VOL[1] and VOL[0] is the 64 kHz clock HZ64K and the output of gate 614 when it is enabled by control signals VOL[1] and VOL[0] is the Boolean product of 64 kHz clock HZ64K and 128 kHz clock HZ128K which is a 64 kHz pulse train of narrower pulse width. As such, the pulse train generation circuit taught by Hsu uses fewer components than the one used by Oprea (Fig. 2). Oprea discloses the desirability of reducing the number of logic gates used in the design (column 1, lines 57-61). Oprea further discloses that any pulse train frequency an order greater than the ringer audio frequency is

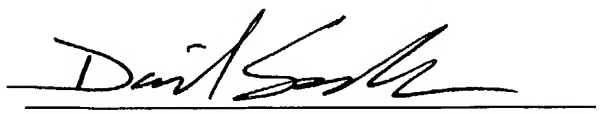
suitable (column 2, lines 10-15). As such, it would have been obvious to one skilled in the art at the time of the invention to apply the 64 kHz pulse train generator taught by Hsu to the combination made obvious by Oprea and Yeh for the purpose of reducing the size, cost and power consumption of the device by reducing the number of logic gates.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel Swerdlow whose telephone number is 703-305-4088. The examiner can normally be reached on Monday through Friday between 8:00 AM and 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Forrester Isen can be reached on 703-305-4386. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Daniel Swerdlow, Patent Examiner Art Unit 2644